Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of providing a modulated signal, the method comprising:

providing a phase modulation signal; and

providing amplitude modulation to the phase modulation signal to generate the modulated signal, wherein the phase modulation and amplitude modulation are synchronized, wherein the modulated signal is provided through to a feedback circuit, the feedback circuit delaying the amplitude modulation in response to the modulated signal to synchronize the phase modulation and the amplitude modulation.

2. (Original) The method of claim 1, wherein the phase modulation and amplitude modulation are synchronized in accordance with a calibration scheme.

3. (Previously Presented) The method of claim 2, wherein the calibration scheme includes providing the modulated signal having a desired characteristic wherein the phase modulation is reversed when the amplitude modulation is minimum.

4. (Currently Amended) The method of claim 3, wherein the calibration scheme utilizes a phase jump detector, an envelope detector, and a minimum detector, the phase jump detector and the envelope detector receiving the modulated signal, the minimum detector receiving an envelope detection signal from the envelope detector to determine the minimum, the phase jump detector determining when the phase modulation is reversed.

5. (Previously Presented) The method of claim 4, wherein the calibration scheme includes detecting a delay between the phase modulation being reversed and the amplitude modulation being minimum.

6. (Original) The method of claim 5, wherein the providing amplitude modulation to the phase modulation signal to generate the modulated signal includes delaying the phase modulation in accordance with the delay.

7. (Original) The method of claim 1, wherein the providing amplitude modulation to the phase modulation signal to generate the modulated signal utilizes a gain controlled amplifier.

8. (Original) The method of claim 1, wherein the modulated signal is a radio frequency signal.

9. (Original) The method of claim 2, wherein the providing a phase modulation signal utilizes a phase lock loop.

10. (Original) The method of claim 9, wherein the providing a phase modulation signal utilizes a sigma-delta controlled phase lock loop.

11. (Currently Amended) A method of modulating first data and second data on a signal, the method comprising steps of:

phase or frequency modulating the signal in accordance with the first data; and

amplitude modulating the signal in accordance with the second data, wherein the steps of phase or frequency modulating and amplitude modulating are coordinated in time with respect to each other to ensure integrity of the first data and the second data, wherein the phase or frequency modulations and amplitude modulations are coordinated in time by delaying the amplitude modulating in response to the signal.

12. (Original) The method of claim 11, wherein a delay circuit is utilized to coordinate in time the phase or frequency modulating step and the amplitude modulating step.

13. (Currently Amended) ~~The method of claim 12~~ A method of modulating first data and second data on a signal, the method comprising steps of:

phase or frequency modulating the signal in accordance with the first data; and

amplitude modulating the signal in accordance with the second data, wherein the steps of phase or frequency modulating and amplitude modulating are coordinated in time with respect to each other to ensure integrity of the first data and the second data, wherein a delay circuit is utilized to coordinate in time the phase or frequency modulating step and the amplitude modulating step, wherein the delay circuit is calibrated by providing the modulated signal having a desired characteristic, the desired characteristic being when the phase modulation is reversed and the amplitude modulation being simultaneously minimum; and detecting a delay between the phase modulation being reversed and the amplitude modulation being minimum.

14. (Currently Amended) A modulator, comprising:

a first data input;

a second data input;

a frequency or phase modulator circuit coupled to the first data input, the frequency or phase modulator circuit providing modulation in response to first data at the first data input; ~~and~~

an amplitude modulator circuit coupled to the second data input, the amplitude modulator circuit providing modulation in response to second data at the second data input wherein a delay circuit is disposed between the second data input and the amplitude modulator circuit, the delay circuit responding to a feedback signal associated with a modulated signal to coordinate the modulation in response to the first data and the modulation in response to the second data.

15. (Original) The modulator of claim 14, further comprising a delay circuit, the delay circuit compensating for time delay for the frequency or phase modulator circuit and the amplitude modulator circuit.

16. (Original) The modulator of claim 14, wherein the amplitude modulator is an amplifier.

17. (Original) The modulator of claim 16, wherein the second data controls power provided to the amplifier.

18. (Original) The modulator of claim 15, wherein the frequency or phase modulator circuit receives an incoming signal and provides a modulated signal to the amplitude modulator circuit.

19. (Original) The modulator of claim 18, wherein the delay circuit is coupled between the second input and the amplitude modulator circuit.

20. (Currently Amended) ~~The modulator of claim 15,~~ A modulator, comprising:

a first data input;

a second data input;

a frequency or phase modulator circuit coupled to the first data input, the frequency or phase modulator circuit providing modulation in response to first data at the first data input;

an amplitude modulator circuit coupled to the second data input, the amplitude modulator circuit providing modulation in response to second data at the second data input; and

a delay circuit, the delay circuit compensating for time delay for the frequency or phase modulator circuit, wherein the amplitude modulator circuit further comprises an envelope detector coupled to the amplitude modulator circuit, a minimum detector coupled to the envelope detector, a phase jump detector coupled to the amplitude modulator circuit, and a phase detector/charge pump circuit coupled to the phase jump detector and the minimum detector, the phase detector/charge pump circuit providing a delay signal during calibration of the modulator.